Amendments to the Specification:

1. Please replace paragraph [0001] with the following amended paragraphs:

[0001] 1. Field of the Invention ~~bk2E001200303263OLE_LINK11. Field of the Inventionbk2E001200303263~~

[0001.1] The present invention relates to a method for fabricating a vertical bipolar junction transistor, and more particularly, to a method for forming a contact region of a vertical bipolar junction transistor by a self-aligned silicidation process (salicide).

2. Please replace paragraph [0002] with the following amended paragraphs:

[0002] 2. Description of the Prior Art ~~bk2E0012003032642. Description of the Prior Artbk2E001200303264~~

[0002.1] Bipolar junction transistors are important elements of a semiconductor. In general, there are two types of bipolar junction transistors: a lateral bipolar junction transistor and a vertical bipolar junction transistor.

3. Please replace paragraph [0005] with the following amended paragraph:

[0005] However, the epitaxial layer of the vertical bipolar junction transistor used for the collector region according to the prior art is normally a thin epitaxial layer 115. In the prior art method for fabricating a

vertical bipolar junction transistor, it is necessary to perform many doping processes and thermal processes through the opening 121 in order to cause the multi-lever structures including the collector enhancement region 123, the base region 125, the emitter region 129, the base contact region 131, and so on formed respectively in the epitaxial layer 115. Thus, precisely controlling the position of the multi-lever structures such as the collector enhancement region [[13]] 123, the base region 125, the emitter region 129, the base contact region131, and so on in the epitaxial layer 115 having limited width and depth is difficult. Furthermore, precisely controlling the concentration of implanted impurities in the above-mentioned multi-lever structures is also difficult after many thermal processes so that the electrical performance of the vertical bipolar junction transistor is greatly affected.

4. Please replace paragraph [0023] with the following amended paragraph:

[0023] As shown in FIG.5, a self-aligned silicidation process can be utilized to form a silicide layer ~~including~~ 230a on the ~~surfaces~~ surface of the doping layer 226, a silicide layer ~~and~~ 230b (230b is shown in Fig.6) on the portion of the third doping region 220 not covered by the doping layer 226, a silicide layer 230c on the ~~surfaces~~ surface of the second doping region 216, and a silicide layer 230d on the ~~surfaces~~ surface of the first doping region 214. The silicide ~~layer functions~~ layers 230a, 230b, 230c, and 230d function as contact regions of the vertical bipolar junction transistor. FIG.6 shows a top view of the metal contact region according to the first embodiment of the present invention. As shown in FIG.6, the self-aligned silicidation process forms the silicide layer 230a on the doping layer 226 to be an emitter contact region ~~230a~~, the silicide layer 230b on

the portion of the third doping region 220 not covered by the doping layer 226 to be a base contact region ~~230b~~, the silicide layer 230c on second doping region 216 to be a collector contact region ~~230c~~, and the silicide layer 230d to be a contact region for other electrical demands. For example, the silicide layer 230d functions as the contact region ~~230d~~ on the surface of the first doping region 214 of the vertical bipolar junction transistor.

5. Please replace paragraph [0030] with the following amended paragraph:

[0030] Next, as shown FIG.11, a self-aligned silicidation process is utilized to form a silicide layer including 430a on the surfaces of the doping layer 426, 430b (not shown in Fig.11), 430c on the surfaces of the heavy doping region 417, and 430d on the surfaces of the first doping region [[214]] 414. The silicide layer functions as contact regions for the vertical bipolar junction transistor.

6. Please replace paragraph [0037] with the following amended paragraph:

[0037] Next, as shown in FIG.16, a self-aligned silicidation process is utilized to form a silicide layer ~~including~~ 530a on the ~~surfaces~~ surface of the doping layer 526, a silicide layer 530b (shown in Fig.17) on the portion of the third doping region 520 not covered by the doping layer 526 and the SAB layer 527, a silicide layer 530c on the ~~surfaces~~ surface of the heavy doping region of P-type 517, and a silicide layer 530d on the ~~surfaces~~ surface of the first doping region 514. The silicide ~~layer functions~~ layers 530a, 530b, 530c, and 530d function as contact regions of the vertical PNP transistor. FIG.17 shows a top view of the metal contact region according to the third embodiment of the present invention. As shown in FIG.17, the self-aligned silicidation process forms the silicide layer 530a on the doping layer 526 to be an emitter contact region ~~530a~~, the silicide layer 530b on

the portion of the third doping region 520 not covered by the doping layer 526 and the SAB layer 527 to be a base contact region ~~530b~~, the silicide layer 530c on the heavy doping region 517 to be a collector contact region 530c, and the silicide layer 530d to be a contact region for other electrical demands. For example, the silicide layer 530d functions ~~,~~ as the contact region ~~530d~~ on the surface of the first doping region of N-type 514 of the vertical PNP transistor.